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-- PROGRAM "Quartus II 64-Bit"

-- VERSION "Version 11.0 Build 157 04/27/2011 SJ Full Version"

-- CREATED "Fri Sep 15 23:41:13 2017"

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

LIBRARY work;

ENTITY praktikum3 IS

PORT

(

a : IN STD\_LOGIC;

b : IN STD\_LOGIC;

c : IN STD\_LOGIC;

d : IN STD\_LOGIC;

pin\_name : OUT STD\_LOGIC

);

END praktikum3;

ARCHITECTURE bdf\_type OF praktikum3 IS

SIGNAL SYNTHESIZED\_WIRE\_0 : STD\_LOGIC;

SIGNAL SYNTHESIZED\_WIRE\_1 : STD\_LOGIC;

SIGNAL SYNTHESIZED\_WIRE\_2 : STD\_LOGIC;

SIGNAL SYNTHESIZED\_WIRE\_3 : STD\_LOGIC;

SIGNAL SYNTHESIZED\_WIRE\_4 : STD\_LOGIC;

SIGNAL SYNTHESIZED\_WIRE\_5 : STD\_LOGIC;

SIGNAL SYNTHESIZED\_WIRE\_6 : STD\_LOGIC;

SIGNAL SYNTHESIZED\_WIRE\_7 : STD\_LOGIC;

BEGIN

SYNTHESIZED\_WIRE\_4 <= SYNTHESIZED\_WIRE\_0 AND c;

SYNTHESIZED\_WIRE\_6 <= SYNTHESIZED\_WIRE\_1 AND SYNTHESIZED\_WIRE\_2;

SYNTHESIZED\_WIRE\_3 <= b AND d;

SYNTHESIZED\_WIRE\_1 <= SYNTHESIZED\_WIRE\_3 OR SYNTHESIZED\_WIRE\_4;

SYNTHESIZED\_WIRE\_7 <= b XOR c;

pin\_name <= SYNTHESIZED\_WIRE\_5 OR SYNTHESIZED\_WIRE\_6;

SYNTHESIZED\_WIRE\_5 <= SYNTHESIZED\_WIRE\_7 AND d;

SYNTHESIZED\_WIRE\_2 <= NOT(a);

SYNTHESIZED\_WIRE\_0 <= NOT(b);

END bdf\_type;